CLAIMS

1. In a transistor device, a gate dielectric comprising:

a first layer comprising hafnium oxide; and

a second layer, adjacent to the first layer, comprising a first metal oxide different from hafnium oxide.

2. The transistor device of claim 1, wherein the gate dielectric is present between a semiconductor substrate and a gate electrode of the transistor device, and wherein the first metal oxide is adjacent to the gate electrode.

3. The transistor device of claim 2, wherein the gate dielectric further comprises a third layer, adjacent to the first layer, comprising a second metal oxide different from hafnium oxide.

4. The transistor device of claim 3, wherein the first metal oxide and the second metal oxide are aluminum oxide.

5. The transistor device of claim 4, wherein the first metal oxide and the second metal oxide are substantially pure aluminum oxide.

6. The transistor device of claim 2, wherein the first metal oxide is amorphous.

7. The transistor device of claim 6, wherein the first metal oxide is aluminum oxide.

8. The transistor device of claim 2, wherein the first metal oxide is zirconium oxide.

9. The transistor device of claim 1, wherein the gate dielectric is present between a semiconductor substrate and a gate electrode of the transistor device, and wherein the first metal oxide is adjacent to the semiconductor substrate.

10. The transistor device of claim 9, wherein the first metal oxide is amorphous.

11. The transistor device of claim 10, wherein the first metal oxide is aluminum oxide.

12. The transistor device of claim 11, wherein the aluminum oxide is substantially pure aluminum oxide.

13. A method of forming a gate dielectric between a gate electrode and a semiconductor substrate, comprising:

depositing a first layer and a second layer adjacent to each other, wherein the first layer comprises hafnium oxide and the second layer comprises a metal oxide different from hafnium oxide.

14. The method of claim 13, wherein the step of depositing is further characterized as forming the metal oxide to be amorphous.

15. The method of claim 14, further comprising forming a transistor device as part of an integrated circuit using the gate dielectric, wherein the step of forming the transistor device is performed at sufficiently low temperatures to prevent crystallization of the metal oxide.

16. The method of claim 15, wherein the metal oxide is aluminum oxide.

17. The method of claim 16, wherein the metal oxide is substantially pure aluminum oxide.

18. The method of claim 17, wherein the step of depositing comprises depositing the second layer on the first layer by ALD.

19. The method of claim 13, wherein the first layer is deposited by CVD and the second layer is only one monolayer of the first metal oxide deposited by ALD.

20. The method of claim 13, wherein the first layer is at least two times thicker than second layer.

21. The method of claim 20, wherein the second layer is zirconium oxide.

22. The method of claim 20, wherein the second layer is substantially pure aluminum oxide.

23. The method of claim 13, further comprising:

depositing a third layer of a second metal oxide on the semiconductor substrate;

wherein the step of depositing comprises:

depositing the first layer on the third layer; and

depositing the second layer on the first layer.

24. The method of claim 23, wherein the second layer comprises substantially pure zirconium oxide.

25. The method of claim 23, wherein the second and third layer comprise substantially pure aluminum oxide.

26. A transistor device, comprising:

a semiconductor substrate having a source, a drain, and a channel between the source and the drain;

a gate electrode over the channel; and

a gate dielectric comprising a first layer of substantially pure hafnium oxide and a second layer, adjacent to the first layer, of a substantially pure metal oxide.

27. The transistor device of claim 26, wherein the gate dielectric further comprises a third layer of the substantially pure metal oxide, wherein the third layer is adjacent to the semiconductor substrate over the channel, the first layer is over the third layer, and the second layer is over the first layer.

28. The transistor device of claim 27, wherein the substantially pure metal oxide is substantially pure amorphous aluminum oxide.

29. The transistor device of claim 26, wherein the second layer is deposited by ALD.

30. The transistor device of claim 29, wherein the second layer is substantially pure zirconium oxide.

31. The transistor device of claim 26, wherein the second layer is substantially pure aluminum oxide.